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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

DINH, TUAN T

ART UNIT

PAPER NUMBER

2827

DATE MAILED: 06/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/955,230

Applicant(s)

KELLY ET AL.

Examiner

Tuan T Dinh

Art Unit

2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 06 February 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-29 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-29 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sehna (U. S. Patent 5,741,729) in view of Jones et al. (U. S. Patent 5,955,704).

As to claim 1, Sehna discloses a printed circuit board (package 50, column 5, line 51) as shown in figures 2-3 comprising:

a signal layer (8A; 8B, column 5, line 53) comprising traces to communicate signals not associated with regulated supply voltage; and

a supply voltage plane (8C, column 3, line 7) embedded in the signal layer (8A; 8B) to supply power of a component (12-figure 2) mounted to the printed circuit board.

Sehna does not disclose the component having a multiple pins connected to the PCB. Jones shows a PCB (28) in figures 2-5 comprising a component (34) having pins (see figure 2) provided a supply power of a component mounted to the PCB.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have teaching's Jones to employ the PCB of Sehna in order to provide a cross-talk protection of a multiplayer circuit board.

As to claims 2-8, 11, Sehna discloses the PCB as shown in figures 2-3 further comprising:

a supply voltage plane layer (60-figure 2; 200; 260-figure 3) separate from the signal layers (8A; 8B), said supply voltage plane layer comprising an embedded ground plane to provide ground connections (see figure 2 and 3) for the signal layer; the supply voltage plane and the ground plane each has an outer boundary, and the ground connections are associated with an electrical device (18) to the component (12).

As to claim 9, Sehna discloses the PCB as shown in figures 2-3 wherein each of the supply voltage plane (8C) and the ground plane (60) lies substantially within a region located directly below the component (12), the component being mounted on top of the signal layer (8A; 8B).

As to claim 10, Sehna discloses the PCB as shown in figures 2-3 wherein the ground plane (60) is significantly larger than the supply voltage plane (8C).

As to claim 12, Sehna discloses the PCB as show in figures 2-3 further comprising:

a core layer (56; 58, column 6, lines 39-41),

wherein the signal layer (8A) and the supply voltage plane layer (8C) are located on the same side of the core layer.

As to claims 13-14, Sehna discloses the PCB as shown in figures 2-3 wherein the voltage plane and the ground plane, each reduces and inductance (column 6, lines 62-67, column 7, lines 1-35)

As to claims 15, 19, Sehna discloses a printed circuit board (package 50, see figures 2-3) comprising:

a supply voltage plane layer (60) to communicate a supply voltage; and

a ground plane (an inner part of Vss plane 60) embedded between the supply voltage plane layer to provide ground connections (by ground vias) of a component (12) mounted to the printed circuit board.

Sehna does not disclose the component having a multiple pins connected to the PCB. Jones shows a PCB (28) in figures 2-5 comprising a component (34) having pins (see figure 2) provided a supply power of a component mounted to the PCB.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have teaching's Jones to employ the PCB of Sehna in order to provide a cross-talk protection of a multilayer circuit board.

As to claim 16, Sehna discloses the PCB as shown in figure 3 further comprising: a ground plane layer (200) separate from the supply voltage plane layer (260).

As to claim 17, Sehna discloses the PCB as shown in figures 2-3 wherein the ground plane lies substantially within a region located directly below the component, the component being mounted on top of the signal layer.

As to claims 18-19, Sehna discloses the PCB as shown in figures 2-3 wherein the ground connections are associated with electrical devices connected to the component, and the ground plane has an outer boundary established by the ground connections.

Regarding claims 20-29, the method is necessitated by the PCB structure as discloses by Sehna in view of Jones.

**Conclusion**


1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Funada and Patil et al. disclose related art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T Dinh whose telephone number is 703-306-5856. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-1341 for regular communications and 703-305-1341 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

TD  
May 30, 2003.

  
DAVID L. TALBOTT  
SUPERVISORY PATENT EXAMINER  
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